# ADCLK925BCPZ

Data Sheet

SiGe ECL Clock/Data Buffers

| | |
|---|---|
| Manufacturers | Analog Devices, Inc |
| Package/Case | LFCSP16 |
| Product Type | Integrated Circuits (ICs) |
| RoHS | |
| Lifecycle | |

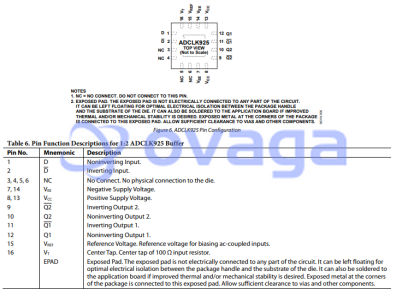


Figure 6. ADCLK925 Pin Configuration

Table 6. Pin Function Descriptions for 1:2 ADCLK925 Buffer

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | D | Noninverting Input. |
| 2 | $\overline{D}$ | Inverting Input. |
| 3, 4, 5, 6 | NC | No Connect. No physical connection to the die. |
| 7, 14 | $V_{EE}$ | Negative Supply Voltage. |
| 8, 13 | $V_{CC}$ | Positive Supply Voltage. |
| 9 | $\overline{Q2}$ | Inverting Output 2. |
| 10 | Q2 | Noninverting Output 2. |
| 11 | $\overline{Q1}$ | Inverting Output 1. |
| 12 | Q1 | Noninverting Output 1. |
| 15 | $V_{REF}$ | Reference Voltage. Reference voltage for biasing ac-coupled inputs. |
| 16 | $V_T$ | Center Tap. Center tap of 100 Ω input resistor. |
| | EPAD | Exposed Pad. The exposed pad is not electrically connected to any part of the circuit. It can be left floating for optimal electrical isolation between the package handle and the substrate of the die. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired. Exposed metal at the corners of the package is connected to this exposed pad. Allow sufficient clearance to vias and other components. |

Images are for reference only

Please submit RFQ for ADCLK925BCPZ or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

## General Description

ADCLK925BCPZ is a high-speed clock buffer designed by Analog Devices, a leading semiconductor manufacturer. Here are some details about this IC:

## Features

Provides 1:2 differential clock outputs

Operating frequency range: DC to 7 GHz

Low additive jitter: 47 fs rms

Low output-to-output skew: 3 ps

Input clock signal can be single-ended or differential

Supports a wide range of input voltage levels (from 0.4V to 2.0V)

Low power consumption: 170 mW at 2.5 GHz

## Application

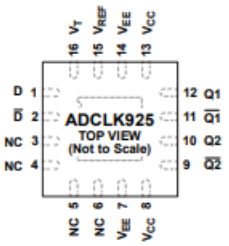
High-speed data communication systems

Test and measurement equipment

Data acquisition systems

Instrumentation and control systems

Medical imaging equipment




NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. EXPOSED PAD. THE EXPOSED PAD IS NOT ELECTRICALLY CONNECTED TO ANY PART OF THE CIRCUIT. IT CAN BE LEFT FLOATING FOR OPTIMAL ELECTRICAL ISOLATION BETWEEN THE PACKAGE HANDLE AND THE SUBSTRATE OF THE DIE. IT CAN ALSO BE SOLDERED TO THE APPLICATION BOARD IF IMPROVED THERMAL AND/OR MECHANICAL STABILITY IS DESIRED. EXPOSED METAL AT THE CORNERS OF THE PACKAGE IS CONNECTED TO THIS EXPOSED PAD. ALLOW SUFFICIENT CLEARANCE TO VIAS AND OTHER COMPONENTS.

*Figure 6. ADCLK925 Pin Configuration*

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## Related Products

ADUM1300

Analog Devices, Inc

ADL5310ACPZ

Analog Devices, Inc

LFCSP-24

ADG5409BCPZ

Analog Devices, Inc

LFCSP-16

ADG3308BCPZ

Analog Devices, Inc

20LFCS

ADR391AUJZ

Analog Devices, Inc

SOT23-5

ADCMP600BKSZ

Analog Devices, Inc

SC-70-5

ADM7171ACPZ

Analog Devices, Inc

LFCSP8

ADCMP601BKSZ

Analog Devices, Inc

SC70