

PIC32MX150F128D-I/PT

Data Sheet

Microcontroller PIC/DSPIC, PIC32 Family PIC32MX Series, 32bit, 40MHz, 128KB, 32KB RAM, TQFP-44

Manufacturers	Microchip Technology, Inc
Package/Case	TQFP-44
Product Type	Embedded Processors & Controllers
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for PI	C32MX150F128D-I/PT (or Email to us: sales@ovaga.con	We will contact yo	u in 12 hours.	RFQ
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General Description

DEVICE OVERVIEW

This document contains device-s PIC32MX1XX/2XX devices.

Operating Conditions

• 2.3V to 3.6V, -40°C to +105°C, DC to 40 MHz

Core: 40 MHz MIPS32® M4K®

- MIPS16e® mode for up to 40% smaller code size
- 1.56 DMIPS/MHz (Dhrystone 2.1) performance
- Code-efficient (C and Assembly) architecture
- Single-cycle (MAC) 32x16 and two-cycle 32x32 multiply

Clock Management

- 0.9% internal oscillator
- Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer
- · Fast wake-up and start-up

Power Management

- Low-power management modes (Sleep, Idle)
- Integrated Power-on Reset and Brown-out Reset
- 0.5 mA/MHz dynamic current (typical)
- 20 µA IPD current (typical)

Timers/Output Compare/Input Capture

- Five General Purpose Timers:
 - Five 16-bit and up to two 32-bit Timers/Counters
- Five Output Compare (OC) modules

Erro Innut Contino (IC) modulos

Ovaga Technologies Limited

- Peripheral Pin Select (PPS) to allow function remap
- Real-Time Clock and Calendar (RTCC) module

Communication Interfaces

- USB 2.0-compliant Full-speed OTG controller
- Two UART modules (10 Mbps)
- Supports LIN 2.0 protocols and IrDA® support
- Two 4-wire SPI modules (20 Mbps)
- Two I2C modules (up to 1 Mbaud) with SMBus support
- Peripheral Pin Select (PPS) to allow function remap
- Parallel Master Port (PMP)

Direct Memory Access (DMA)

- · Four channels of hardware DMA with automatic data size detection
- Two additional channels dedicated for USB
- Programmable Cyclic Redundancy Check (CRC)

Input/Output

- 15 mA source/sink on all I/O pins
- 5V-tolerant pins
- · Selectable open drain, pull-ups, and pull-downs
- External interrupts on all I/O pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 2 -40°C to +105°C) planned
- Class B Safety Library, IEC 60730

Debugger Development Support

- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited program and six complex data breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan

Features

Microcontroller Features

Peripheral Features

Audio Interface Features

Analog Features

Debug Features



Related Products



PIC24F16KA101-I/SS

Microchip Technology, Inc SSOP-20

PIC16F1938-I/SP Microchip Technology, Inc PDIP-28



PIC18F6520-I/PT

Microchip Technology, Inc TQFP-64



Microchip Technology, Inc SOIC-28









PIC16F1936-I/SS

Microchip Technology, Inc SSOP-28

PIC18F23K22-I/SP

Microchip Technology, Inc SPDIP-28

PIC18F2620-I/SP

Microchip Technology, Inc SPDIP-28

PIC18F97J60T-I/PT

Microchip Technology, Inc **TQFP-100**

