

PLL Clock Generator, 1.25 GHz, 3.135V-3.465V supply, 14 Outputs, LFCSP-72

Manufacturers	Analog Devices, Inc
Package/Case	72-VFQFN, CSP
Product Type	Clock & Timer ICs
RoHS	Green
Lifecycle	



Images are for reference only

Please submit RFQ for AD9528BCPZ or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

General Description

The AD9528 is a two-stage PLL with an integrated JESD204BSYSREF generator for multiple device synchronization. The first stage phase-locked loop (PLL) (PLL1) provides input reference conditioning by reducing the jitter present on a system clock. The second stage PLL (PLL2) provides high frequency clocks that achieve low integrated jitter as well as low broadband noise from the clock output drivers. The external VCXO provides the low noise reference required by PLL2 to achieve the restrictive phase noise and jitter requirements necessary to achieve acceptable performance. The on-chip VCO tunes from 3.450 GHz to 4.025 GHz. The integrated SYSREF generator outputs single shot, N-shot, or continuous signals synchronous to the PLL1 and PLL2 outputs to time align multiple devices.

The AD9528 generates six outputs (Output 0 to Output 3, Output 12, and Output 13) with a maximum frequency of 1.25 GHz, and eight outputs with a maximum frequency of up to 1 GHz. Each output can be configured to output directly from PLL1, PLL2, or the internal SYSREF generator. Each of the 14 output channels contains a divider with coarse digital phase adjustment and an analog fine phase delay block that allows complete flexibility in timing alignment across all 14 outputs. The AD9528 can also be used as a dual input flexible buffer to distribute 14 device clock and/or SYSREF signals. At power-up, the AD9528 sends the VCXO signal directly to Output 12 and Output 13 to serve as the power-up ready clocks.

Features

- 14 outputs configurable for HSTL or LVDS
- Maximum output frequency
- 6 outputs up to 1.25 GHz
- 8 outputs up to 1 GHz
- Dependent on the voltage controlled crystal oscillator
- Dedicated 8-bit dividers on each output
- Coarse delay: 63 steps at 1/2 the period of the RF VCO divider output frequency

Application

- High performance wireless transceivers
- LTE and multicarrier GSM base stations
- Wireless and broadband infrastructure
- Medical instrumentation
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs; supports JESD204B
- Low jitter, low phase noise clock distribution

with no jitter impact

ATE and high performance instrumentation

Fine delay: 15 steps of 31 ps resolution

Typical output to output skew: 20 ps

Duty cycle correction for odd divider settings

Output 12 and Output 13, VCXO output at power-up

Absolute output jitter: <160 fs at 122.88 MHz, 12 kHz to 20 MHz integration range

Digital frequency lock detect

SPI- and I2C-compatible serial control port

Dual PLL architecture

PLL1

Provides reference input clock cleanup with external VCXO

Phase detector rate up to 110 MHz

Redundant reference inputs

Automatic and manual reference switchover modes Revertive and nonrevertive switching

Loss of reference detection with holdover mode

Low noise LVDS/HSTL outputs from VCXO used for radio frequency/intermediate frequency (RF/IF) synthesizers

PLL2

Phase detector rate of up to 275 MHz

Integrated low noise VCO



Related Products



[ADF4350BCPZ](#)

Analog Devices, Inc
LFCSP-32



[AD9516-4BCPZ](#)

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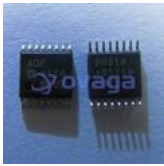
[ADF4111BRUZ](#)

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