

## CMOS ARINC Bus Interface Circuit

Manufacturers	<a href="#">Renesas Technology Corp</a>
Package/Case	LCC-44
Product Type	Interface ICs
RoHS	
Lifecycle	



Images are for reference only

Please submit RFQ for HS4-3282-8 or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com). We will contact you in 12 hours.

[RFQ](#)

## General Description

The HS-3282 is a high performance CMOS bus interface circuit that is intended to meet the requirements of ARINC Specification 429, and similar encoded, time multiplexed serial data protocols. This device is intended to be used with the HS-3182, a monolithic DI bipolar differential line driver designed to meet the specifications of ARINC 429. The ARINC 429 bus interface circuit consists of two (2) receivers and a transmitter operating independently as shown in Figure 1. The two receivers operate at a frequency that is ten (10) times the receiver data rate, which can be the same or different from the transmitter data rate. Although the two receivers operate at the same frequency, they are functionally independent and each receives serial data asynchronously. The transmitter section of the ARINC bus interface circuit consists mainly of a First-In First-Out (FIFO) memory and timing circuit. The FIFO memory is used to hold up to eight (8) ARINC data words for transmission serially. The timing circuit is used to correctly separate each ARINC word as required by ARINC Specification 429. Even though ARINC Specification 429 specifies a 32-bit word, including parity, the HS-3282 can be programmed to also operate with a word length of 25 bits. The incoming receiver data word parity is checked, and a parity status is stored in the receiver latch and output on Pin BD08 during the 1st word. [A logic "0" indicates that an odd number of logic "1"s were received and stored; a logic "1" indicates that an even number of logic "1"s were received and stored]. In the transmitter the parity generator will generate either odd or even parity depending upon the status of PARCK control signal. A logic "0" on BD12 will cause odd parity to be used in the output data stream. Versatility is provided in both the transmitter and receiver by the external clock input which allows the bus interface circuit to operate at data rates from 0 to 100 kilobits. The external clock must be ten (10) times the data rate to insure no data ambiguity. The ARINC bus interface circuit is fully guaranteed to support the data rates of ARINC specification 429 over both the voltage ( $\pm 5\%$ ) and full military temperature range. It interfaces with UL, CMOS or NMOS support circuitry, and uses the standard 5-volt VCC supply.

## Features

ARINC Specification 429 Compatible

Data Rates of 100 Kilobits or 12.5 Kilobits

Separate Receiver and Transmitter Section

Dual and Independent Receivers, Connecting Directly to ARINC Bus

Serial to Parallel Receiver Data Conversion

Parallel to Serial Transmitter Data Conversion

Word Lengths of 25 or 32 Bits

Parity Status of Received Data

Generate Parity of Transmitter Data

Automatic Word Gap Timer

Single 5V Supply

Low Power Dissipation

Full Military Temperature Range





## Related Products



### [HS1-3282-8](#)

Renesas Technology Corp  
CDIP-40



### [HS1-3182-8](#)

Renesas Technology Corp  
DIP16



### [HI9P0201HS-5Z](#)

Renesas Technology Corp  
SOIC-16



### [HI3-0201HS-5Z](#)

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CDIP-16



### [HI9P0201HS-9Z](#)

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### [HS1-3182-9+](#)

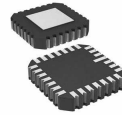
Renesas Technology Corp  
16-CDIP (0.300, 7.62mm)



[HI1-0201HS-2](#)

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[HS4-3182-8](#)

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