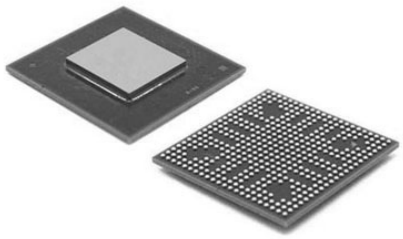
AD9129BBCZ

Data Sheet

Digital to Analog Converters - DAC 14-Bit 5.6 GSPS RF

Manufacturers	Analog Devices, Inc
Package/Case	64LFCSP
Product Type	Data Conversion ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for AD9129BBCZ or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The AD9119/AD9129 are high performance, 11-/14-bit RF digital-to-analog converters (DACs) supporting data rates up to 2.85 GSPS. The DAC core is based on a quad-switch architecture that enables dual-edge clocking operation, effectively increasing the DAC update rate to 5.7 GSPS when configured for Mix-Mode™ or 2× interpolation. The high dynamic range and bandwidth enable multicarrier generation up to 4.2 GHz.

In baseband mode, wide bandwidth capability combines with high dynamic range to support from 1 to 158 contiguous carriers for CATV infrastructure applications. A choice of two optional 2× interpolation filters is available to simplify the postreconstruction filter by effectively increasing the DAC update rate by a factor of 2. In Mix-Mode operation, the AD9119/AD9129 can reconstruct RF carriers in the second and third Nyquist zone while still maintaining exceptional dynamic range up to 4.2 GHz. The high performance NMOS DAC core features a quad-switch architecture that enables industry-leading direct RF synthesis performance with minimal loss in output power. The output current can be programmed over a range of 9.5 mA to 34.4 mA.

The AD9119/AD9129 include several features that may further simplify system integration. A dual-port, source synchronous LVDS interface simplifies the data interface to a host FPGA/ASIC. A differential frame/parity bit is also included to monitor the integrity of the interface. On-chip delay locked loops (DLLs) optimize timing between different clock domains.

A serial peripheral interface (SPI) configures the AD9119/ AD9129 and monitors the status of readback registers. The AD9119/AD9129 are manufactured on a 0.18 µm CMOS process and operates from +1.8 V and −1.5 V supplies. It is supplied in a 160-ball chip scale package ball grid array.

Product Highlights

High dynamic range and signal reconstruction bandwidth support RF signal synthesis of up to 4.2 GHz.

Dual-port interface with double data rate (DDR) LVDS data receivers supports 2850 MSPS maximum conversion rate.

Manufactured on a CMOS process; a proprietary switching technique enhances dynamic performance.

Features

DAC update rate: up to 5.7 GSPS

Direct RF synthesis at 2.85 GSPS data rate

DC to 1.425 GHz in baseband mode

DC to 1.0 GHz in 2× interpolation mode

1.425 GHz to 4.2 GHz in Mix-Mode

Bypassable 2× interpolation

Excellent dynamic performance

Supports DOCSIS 3.0 wideband ACLR/harmonic performance

8 QAM carriers: ACLR > 65 dBc

Industry-leading single/multicarrier IF or RF synthesis

4-carrier W-CDMA ACLR at 2457.6 = 71 dBc (baseband = 68 dBc = 67 dBc (Mix-Mode)

Dual-port LVDS and DHSTL data interface

Up to 1.425 GSPS operation

Source synchronous DDR clocking with parity bit

Low power: 1.0 W at 2.85 GSPS (1.3 W at 5.7 GSPS

Application

Broadband communications systems

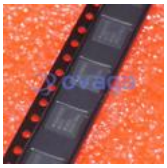
CMTS/VOD

Wireless infrastructure: W-CDMA, LTE, point-to-point

Instrumentation, automatic test equipment (ATE)

Radar, jammers

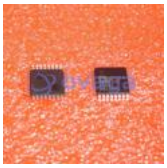
Related Products



ADAS3022BCPZ

Analog Devices, Inc

LFCSP-40



AD7266BSUZ

Analog Devices, Inc

TQPF-32

AD574AJNZ

Analog Devices, Inc

PDIP-28

AD7401YRWZ

Analog Devices, Inc

SOIC-16

AD7938BSUZ

Analog Devices, Inc

TQFP-32

AD7192BRUZ-REEL

Analog Devices, Inc

TSSOP-24

AD7124-8BCPZ-RL7

Analog Devices, Inc

LFCSP-32

AD9680BCPZ-500

Analog Devices, Inc

LFCSP-64