

Clock Generator 300MHz to 3.5GHz Input 470MHz Output 32Pin LFCSP EP Tray

Manufacturers	<a href="#">Analog Devices, Inc</a>
Package/Case	LFCSP-32
Product Type	Clock/Timing - Clock Generators, PLLs, Frequency Synthesizers
RoHS	Green
Lifecycle	



Images are for reference only

Please submit RFQ for ADF4193BCPZ or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

## General Description

The ADF4193 frequency synthesizer can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. Its architecture is specifically designed to meet the GSM/EDGE lock time requirements for base stations. It consists of a low noise, digital phase frequency detector (PFD), and a precision differential charge pump. There is also a differential amplifier to convert the differential charge pump output to a single-ended voltage for the external voltage-controlled oscillator (VCO).

The  $\Sigma$ - $\Delta$ -based fractional interpolator, working with the N divider, allows programmable modulus fractional-N division. Additionally, the 4-bit reference (R) counter and on-chip frequency doubler allow selectable reference signal (REFIN) frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and a VCO. The switching architecture ensures that the PLL settles inside the GSM time slot guard period, removing the need for a second PLL and associated isolation switches. This decreases cost, complexity, PCB area, shielding, and characterization on previous ping-pong GSM PLL architectures.

## Features

New, fast settling, fractional-N PLL architecture

Single PLL replaces ping-pong synthesizers

Frequency hop across GSM band in 5  $\mu$ s with phase settled by 20  $\mu$ s

0.5° rms phase error at 2 GHz RF output

Digitally programmable output phase

RF input range up to 3.5 GHz

3-wire serial interface

On-chip, low noise differential amplifier

Phase noise figure of merit: -216 dBc/Hz

Loop filter design possible using ADIsimPLL™

Qualified for automotive applications

## Application

GSM/EDGE base stations

PHS base stations

Instrumentation and test equipment





## Related Products



### [ADF4350BCPZ](#)

Analog Devices, Inc  
LFCSP-32



### [AD9516-4BCPZ](#)

Analog Devices, Inc  
LFCSP64



### [ADF4111BRUZ](#)

Analog Devices, Inc  
TSSOP-16



### [ADF4113BRUZ](#)

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### [ADF4116BRUZ](#)

Analog Devices, Inc  
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### [ADF4110BRUZ](#)

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### [AD2S99BPZ](#)

Analog Devices, Inc  
PLCC-20



### [AD9528BCPZ](#)

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72-VFQFN, CSP