

2-Channel Dual ADC Pipelined 500MSPs 14-bit Serial 64-Pin LFCSP EP Tray

Manufacturers	Analog Devices, Inc
Package/Case	LFCSP-64
Product Type	Data Conversion ICs
RoHS	Pb-free Halide free
Lifecycle	



Images are for reference only

Please submit RFQ for AD9680BCPZ-500 or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

General Description

The AD9680 is a dual, 14-bit, 1.25 GSPS/1 GSPS/820 MSPS/500 MSPS analog-to-digital converter (ADC). The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use. This device is designed for sampling wide bandwidth analog signals of up to 2 GHz. The AD9680 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The analog input and clock signals are differential inputs. Each ADC data output is internally connected to two digital down-converters (DDCs). Each DDC consists of up to five cascaded signal processing stages: a 12-bit frequency translator (NCO), and four half-band decimation filters. The DDCs are bypassed by default.

In addition to the DDC blocks, the AD9680 has several functions that simplify the automatic gain control (AGC) function in the communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-, two-, or four-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9680 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V to 3.3 V capable, 3-wire SPI.

The AD9680 is available in a Pb-free, 64-lead LFCSP and is specified over the -40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

APPLICATIONS

Wide full power bandwidth supports IF sampling of signals up to 2 GHz.

Buffered inputs with programmable input termination eases filter design and implementation.

Four integrated wideband decimation filters and numerically controlled oscillator (NCO) blocks supporting multiband receivers.

Flexible serial port interface (SPI) controls various product features and functions to meet specific system requirements.

Programmable fast overrange detection.

9 mm × 9 mm, 64-lead LFCSP.

Features

JESD204B (Subclass 1) coded serial digital outputs

1.65 W total power per channel at 1 GSPS (default settings)

SFDR at 1>

SNR at 1>>>>

Flexible input range: 1.46 V

p-p

p-p

AD9680-1250: 1.58 V

p-p

AD9680-1000 and AD9680-820: 1.70 V p-p nominal

AD9680-500: 1.46 V

p-p

p-p

p-p

AD9680-1250: 1.58 V

p-p

AD9680-1000 and AD9680-820: 1.70 V p-p nominal

AD9680-500: 1.46 V

p-p

Application

Communications

Diversity multiband, multimode digital receivers

3G/4G, TD-SCDMA, W-CDMA, GSM, LTE

General-purpose software radios

Ultrawideband satellite receivers

Instrumentation

Radars

Signals intelligence (SIGINT)

DOCSIS 3.0 CMTS upstream receive paths

HFC digital reverse path receivers

3G/4G, TD-SCDMA, W-CDMA, GSM, LTE

p-p

p-p

Noise>

1.25 V, 2.5 V, and 3.3 V dc supply operation

No missing codes

Internal ADC voltage reference

Programmable termination impedance

400 Ω , 200 Ω , 100 Ω , and 50 Ω differential

2 GHz usable analog input full power bandwidth

95 dB channel isolation/crosstalk

Amplitude detect bits for efficient AGC implementation

2 integrated wideband digital processors per channel

12-bit NCO, up to 4 half-band filters

Differential clock input

Integer clock divide by 1, 2, 4, or 8

Flexible JESD204B lane configurations

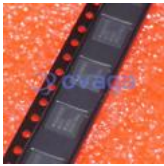
Small signal dither

400 Ω , 200 Ω , 100 Ω , and 50 Ω differential

12-bit NCO, up to 4 half-band filters



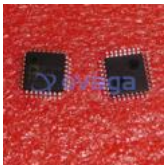
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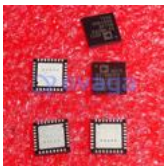
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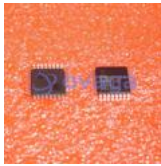
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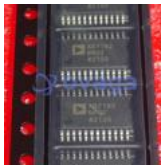
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